

## **LISTING OF THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended) Apparatus for indirectly sensing the temperature of a power MOS device comprising:

a power MOS device having a current sense circuit for sensing a current in the power MOS device;

a circuit for producing a voltage related to a drain-source voltage of the power MOS device;

a comparator coupled to receive at a first input the voltage related to the drain-source voltage of the power MOS device and at a second input a voltage related to the current in the power MOS device;

the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs, the comparator generating the overtemperature protection signal when the temperature of the power MOS device has exceeded a predetermined level determined by the predetermined inequality.

Claim 2 (Previously Presented) The apparatus of claim 1, wherein the predetermined inequality is that the voltage at the first input of the comparator exceeds the voltage at the second input.

Claim 3 (Previously Presented) The apparatus of claim 1, wherein the predetermined inequality is that the voltage at the second input of the comparator exceeds the voltage at the first input.

Claim 4 (Previously Presented) Apparatus for indirectly sensing the temperature of a power MOS device comprising:

a power MOS device having a current sense circuit for sensing a current in the power MOS device;

a circuit for producing a voltage related to a drain-source voltage of the power MOS device;

a comparator coupled to receive at a first input the voltage related to the drain-source voltage of the power MOS device and at a second input a voltage related to the current in the power MOS device;

the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs,

wherein the circuit for producing a voltage related to the drain-source voltage comprises a voltage divider coupled between the drain and source of the power MOS device.

Claim 5 (Previously Presented) The apparatus of claim 4, wherein the power MOS device has a main current cell and a current sense cell, the current sense cell comprising the current sense circuit, and the voltage divider is coupled between the drain and source of the main current cell.

Claim 6 (Previously Presented) The apparatus of claim 5, wherein the comparator has the first input connected to an output of the voltage divider and the second input coupled to the source of the current sense cell.

Claim 7 (Previously Presented) The apparatus of claim 4, wherein the voltage divider comprises first and second resistors with an output coupled to the first input of the comparator.

Claim 8 (Previously Presented) The apparatus of claim 7, wherein the current sense cell is coupled in series with a resistor, the current sense cell and resistor being coupled

across the main current cell, a common connection of the current sense cell and the resistor being coupled to the second input of the comparator.

- Claim 9 (Previously Presented) The apparatus of claim 6, wherein the first input to the comparator comprises a non-inverting input and the second input comprises an inverting input.
- Claim 10 (Previously Presented) The apparatus of claim 8, wherein the resistor comprises a precision resistor.
- Claim 11 (Previously Presented) The apparatus of claim 8, further comprising a second comparator coupled across said resistor for providing a signal indicative of a short circuit condition.
- Claim 12 (Previously Presented) The apparatus of claim 1, wherein the circuit for producing a voltage related to the drain-source voltage of the power MOS device comprises a current mirror circuit and a resistor in series with the current mirror circuit, the resistor generating a voltage related to the current in the power MOS device.
- Claim 13 (Previously Presented) The apparatus of claim 12, wherein the power MOS device has a main current cell and a current sense cell, further comprising a pair of transistors each having a control electrode driven by an amplifier, the amplifier having inputs coupled respectively to the sources of the main current cell and current sense cell of the power MOS device and wherein a predetermined current ratio exists between the currents in the pair of transistors, one of said transistors providing a reduced current related to the current in the power MOS device to the current mirror.

- Claim14 (Previously Presented) The apparatus of claim 13, wherein the comparator has its non-inverting input coupled to a common connection of said resistor and current mirror and its inverting input coupled to the source of the main cell of the power MOS device.
- Claim 15 (Previously Presented) Apparatus for indirectly sensing the temperature of a power MOS device comprising:
- a power MOS device having a current sense circuit for sensing the current in the power MOS device;
  - a voltage divider coupled between the drain and source of the power MOS device;
  - a comparator coupled to receive at a first input an output of the voltage divider and at a second input a voltage related to the current in the power MOS device;
  - the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs.
- Claim 16 (Previously Presented) The apparatus of claim 15, wherein the predetermined inequality is that the voltage at the first input of the comparator exceeds the voltage at the second input.
- Claim 17 (Previously Presented) The apparatus of claim 15, wherein the power MOS device has a main current cell and a current sense cell, the current sense cell comprising the current sense circuit, and the voltage divider is coupled between the drain and source of the main current cell.

- Claim 18 (Previously Presented) The apparatus of claim 17, wherein the comparator has the first input connected to an output of the voltage divider and the second input coupled to the source of the current sense cell.
- Claim 19 (Previously Presented) The apparatus of claim 17, wherein the voltage divider comprises first and second resistors with an output coupled to the first input of the comparator.
- Claim 20 (Previously Presented) The apparatus of claim 19, wherein the current sense cell is coupled in series with a resistor, the current sense cell and resistor being coupled across the main current cell, a common connection of the current sense cell and the resistor being coupled to the second input of the comparator.
- Claim 21 (Previously Presented) The apparatus of claim 20, wherein the resistor comprises a precision resistor.
- Claim 22 (Previously Presented) The apparatus of claim 20, further comprising a second comparator coupled across said resistor for providing a signal indicative of a short circuit condition.
- Claim 23 (Currently Amended) Apparatus for indirectly sensing the temperature of a power MOS device comprising:
- a power MOS device having a current sense circuit for sensing the current in the power MOS device, wherein the current sense circuit includes a circuit for providing a voltage related to the current in the power MOS device from the sensed current;
  - a comparator coupled to receive at a first input a voltage related to the voltage across the drain and source of the power MOS device and at a second input the voltage related to the current in the power MOS device;

the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs, the comparator generating the overtemperature protection signal when the temperature of the power MOS device has exceeded a predetermined level determined by the predetermined inequality..

- Claim 24 (Previously Presented) The apparatus of claim 23 wherein the predetermined inequality is that the voltage at the second input of the comparator exceeds the voltage at the first input.
- Claim 25 (Previously Presented) The apparatus of claim 23 wherein the power MOS device has a main current cell and a current sense cell, the current sense cell comprising the current sense circuit and the current sense circuit provides a current to a current mirror circuit and a resistor for providing a voltage across the resistor related to the current in the power MOS device.
- Claim 26 (Previously Presented) The apparatus of claim 25 wherein the circuit for providing a voltage related to the current in the power MOS device further comprises first and second transistors for providing a reduced current proportional to the current in the current sense circuit.
- Claim 27 (Previously Presented) The apparatus of claim 26 further wherein the current mirror circuit provides a current proportional to the current in the current sense circuit and wherein the current proportional to the current in the current sense circuit flows through said resistor which develops a voltage that is applied to the second input of the comparator.
- Claim 28 (Previously Presented) The apparatus of claim 27, wherein the first input of the comparator is an inverting input and the second input is a non-inverting input.

- Claim 29 (Previously Presented) The apparatus of claim 27 further comprising an amplifier having first and second inputs coupled respectively to the source of the main current cell of the power MOS device and the current sense cell of the power MOS device for driving said first and second transistors.
- Claim 30 (Currently Amended) A method for indirectly sensing the temperature of a power MOS device comprising:
- sensing a first voltage related to the drain-source voltage of the power MOS device;
  - sensing a second voltage related to the current in the power MOS device;
  - comparing the first and second voltages; and
  - generating an overtemperature protection signal when a predetermined inequality between the first and second voltages occurs when the temperature of the power MOS device has exceeded a predetermined level determined by the predetermined inequality.
- Claim 31 (Previously Presented) The method of claim 30, wherein the predetermined inequality is that the first voltage exceeds the second voltage.
- Claim 32 (Previously Presented) The method of claim 30, wherein the predetermined inequality is that the second voltage exceeds the first voltage.
- Claim 33 (Previously Presented) The method of claim 30, wherein the step of sensing the first voltage comprises sensing a voltage related to a voltage dropped by a main current cell of the power MOS device.
- Claim 34 (Previously Presented) A method for indirectly sensing the temperature of a power MOS device comprising:

sensing a first voltage related to the drain-source voltage of the power MOS device;

sensing a second voltage related to the current in the power MOS device;  
comparing the first and second voltages; and

generating an overtemperature protection signal when a predetermined inequality between the first and second voltages occurs,

wherein the step of sensing the first voltage comprises sensing a first voltage from a resistor voltage divider coupled across the drain-source path of the power MOS device.

Claim 35 (Previously Presented) The method of claim 34, further comprising sensing the second voltage by sensing a voltage across a resistor coupled in series with the current sense cell, the current sense cell and resistor being coupled across a main current cell of the power MOS device..

Claim 36 (Previously Presented) The method of claim 35, wherein the step of sensing the second voltage comprises sensing the second voltage across a resistor comprising a precision resistor.

Claim 37 (Previously Presented) The method of claim 35, further comprising comparing the voltage across said resistor for providing a signal indicative of a short circuit condition.

Claim 38 (Previously Presented) The method of claim 33, wherein the step of sensing the second voltage comprises sensing a voltage across a resistor proportional to the current in the power MOS device.